

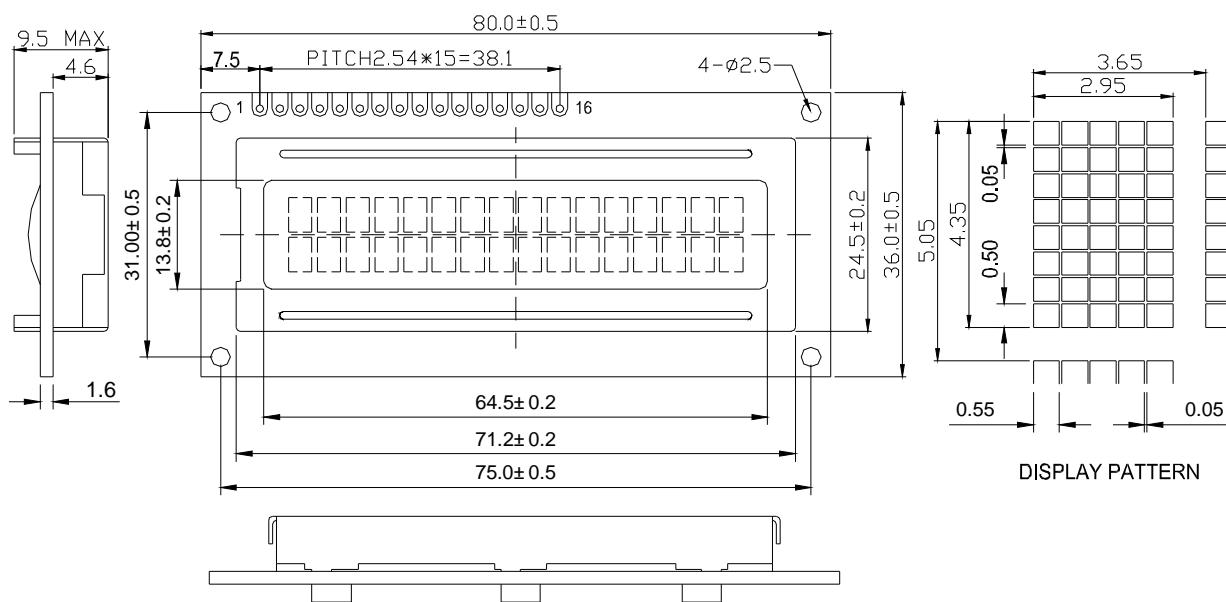
## GDM1602A-NS(YG)-BTS

## SPECIFICATIONS OF LCD MODULE

### 1、Features

1. 5x7 dots with cursor
2. Built-in controller (ST7066U-0A or equivalent)
3. +5V power supply
4. Easy interface with 4-bit or 8-bit MPU
5. Display Mode: STN(blue), Transmissive, Negative
6. Viewing angle: 12:00 O'clock
7. Side BKL(Yellow-Green) to be driven by pin15, pin16

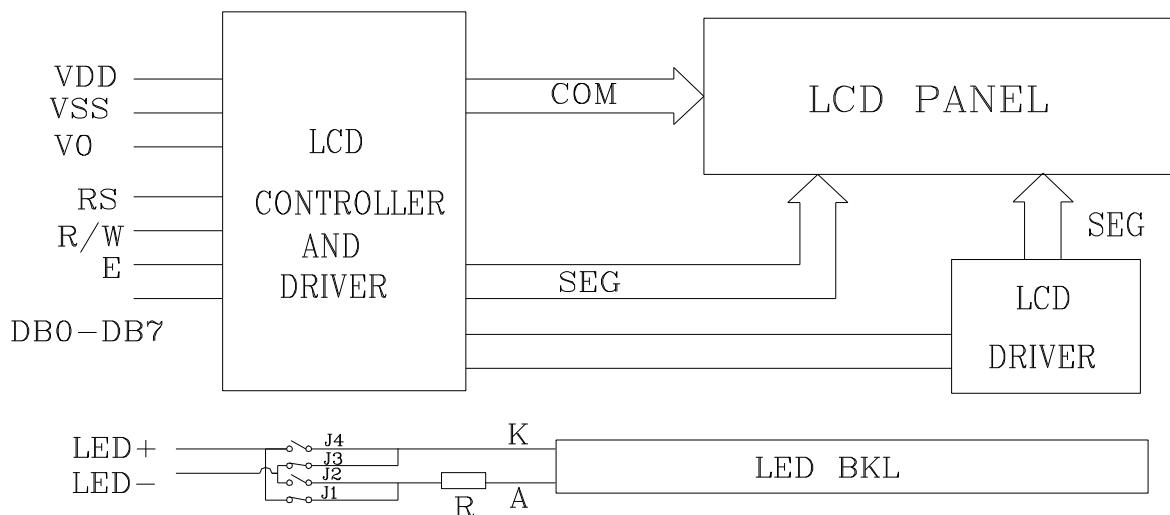
### 2、Outline dimension



### 3、Absolute maximum ratings

Item	Symbol	Standard			Unit
Power voltage	$V_{DD}-V_{SS}$	0	-	7.0	V
Input voltage	$V_{in}$	$V_{SS}$	-	$V_{DD}$	
Operating temperature range	$V_{op}$	0	-	+50	
Storage temperature range	$V_{st}$	-20	-	+60	

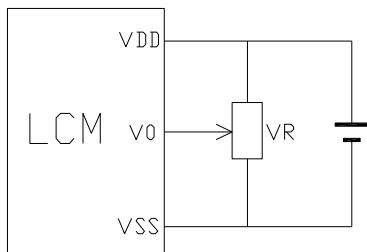
## 4、Block diagram



## 5、Interface pin description

Pin no.	Symbol	External connection	Function
1	$V_{SS}$	Power supply	Signal ground for LCM (GND)
2	$V_{DD}$		Power supply for logic (+5.0V) for LCM
3	$V_0$		Contrast adjust
4	RS	MPU	Register select signal
5	R/W	MPU	Read/write select signal
6	E	MPU	Operation (data read/write) enable signal
7~10	DB0~DB3	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.
11~14	DB4~DB7	MPU	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU
15	LED+	LED BKL power supply	Power supply for BKL
16	LED-		Power supply for BKL (GND)

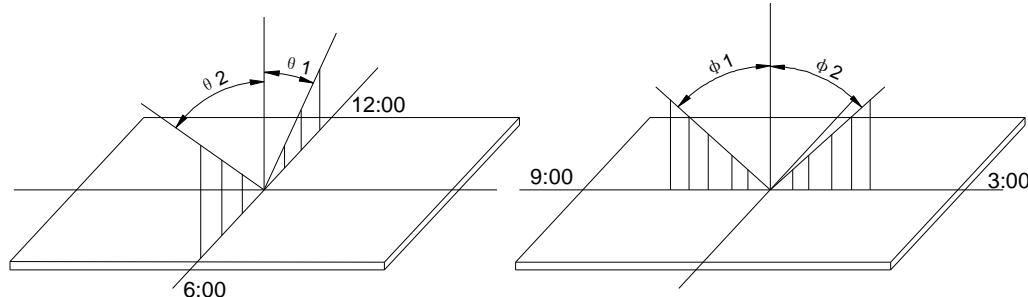
## 6、Contrast adjust



$V_{DD-V_0}$ : LCD Driving voltage

VR: 10k~20k

## 7.Optical characteristics



STN type display module (Ta=25°C, VDD=5.0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ 1	Cr ≥ 3		40		deg
	θ 2			20		
	Φ 1			35		
	Φ 2			35		
Contrast ratio	Cr		-	10	-	-
Response time (rise)	Tr	-	-	200	250	ms
Response time (fall)	Tr	-	-	300	350	

## 8.Electrical characteristics

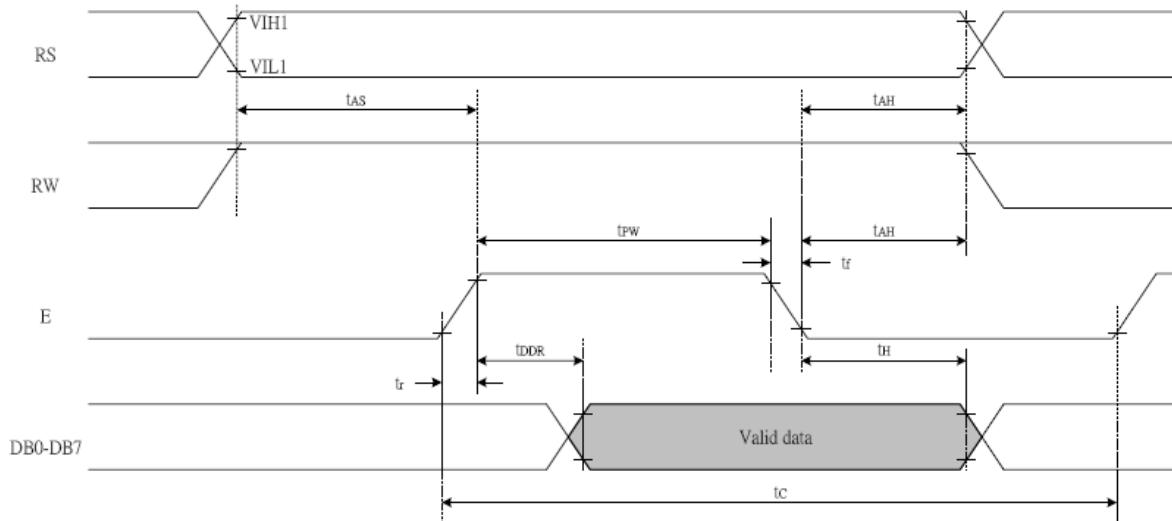
### DC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	V <sub>DD</sub> -V <sub>0</sub>	Ta =25°C	4.0	4.3	4.6	V
Input voltage	V <sub>DD</sub>		4.5	5.0	5.5	
Supply current	I <sub>DD</sub>	Ta=25°C, V <sub>DD</sub> =5.0V	-	1.5	2.5	mA
Input leakage current	I <sub>LKG</sub>		-	-	1.0	uA
“H” level input voltage	V <sub>IH</sub>		0.7V <sub>DD</sub>	-	V <sub>DD</sub>	V
“L” level input voltage	V <sub>IL</sub>	Twice initial value or less	-0.3	-	0.6	
“H” level output voltage	V <sub>OH</sub>	LOH=-0.1mA	3.9	-	V <sub>DD</sub>	
“L” level output voltage	V <sub>OL</sub>	LOH=0.1mA	-	-	0.4	
Backlight supply Current	I <sub>F</sub>	V <sub>LED+</sub> = 5.0V R=51Ω	-	20	-	mA

Read cycle (Ta=25°C, VDD=5.0V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	t <sub>c</sub>	E	1200	-	-	ns
Enable pulse width	t <sub>pw</sub>		140	-	-	
Enable rise/fall time	t <sub>r, tf</sub>		-	-	25	
Address setup time	t <sub>as</sub>		0	-	-	
Address hold time	t <sub>ah</sub>	RS; R/W,E	10	-	-	
Data setup delay	t <sub>ddr</sub>	DB0~DB7	-	-	100	
Data hold time	t <sub>h</sub>		10	-	-	

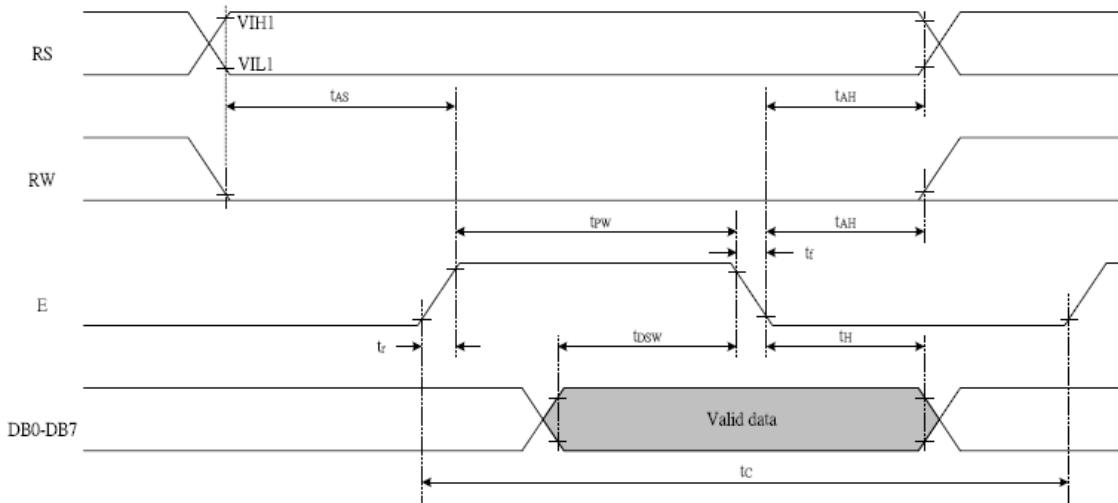
## Read mode timing diagram



**Write cycle (Ta=25°C, VDD=5.0V)**

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	$t_c$	E	1200	-	-	ns
Enable pulse width	$t_{pw}$		140	-	-	
Enable rise/fall time	$t_r, t_f$		-	-	25	
Address setup time	$t_{as}$		0	-	-	
Address hold time	$t_{ah}$	RS; R/W,E	10	-	-	
Data setup delay	$t_{dsd}$	DB0~DB7	40	-	-	
Data hold time	$t_h$		10	-	-	

## Write mode timing diagram



## 9. FUNCTION DESCRIPTION

### Ø System Interface

This chip has all two kinds of interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

### Ø Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not high.

**Ø Address Counter (AC)**

Address Counter (AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 - DB6 ports.

**Ø Display Data RAM (DDRAM)**

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number.

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
DDRAM address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

**Ø CGROM (Character Generator ROM)**

CGROM has a 5 x 8 dots 204 characters pattern and a 5 x 10 dots 32 characters pattern. CGROM has 204 character patterns of 5 x 8 dots.

**Ø CGRAM (Character Generator RAM)**

CGRAM has up to 5 x 8 dot, 8 characters. By writing font data to CGRAM, user defined characters can be used.

Character Code (DDRAM Data)								CGRAM Address					Character Patterns (CGRAM Data)									
b8	b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	-	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-		
0	0	0	0	0	-	0	0	1	0	0	0	0	0	-	-	-	-	-	-	-		

Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

**Notes:**

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
- “-“. Indicates no effect.

**Ø Cursor/Blink Control Circuit**

It controls cursor/blink ON/OFF at cursor position.

## 10. Instruction description

### Outline

To overcome the speed difference between the internal clock of ST7066U and the MPU clock, ST7066U performs internal operations by storing control in formations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table7).

Instructions can be divided largely into four groups:

- 1) ST7066U function set instructions (set display methods, set data length, etc.)
- 2) Address set instructions to internal RAM
- 3) Data transfer instructions with internal RAM
- 4) Others

The address of the internal RAM is automatically increased or decreased by 1.

Note: during internal operation, busy flag (DB7) is read “High”.

Busy flag check must be preceded by the next instruction.

### Instruction Table

Instruction	Instruction code											Description	Execution time (fosc= 270 KHZ)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRA and set DDRAM address to “00H” from AC	1.53ms	
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to “00H” From AC and return cursor to Its original position if shifted. The contents of DDRAM are not changed.	1.53ms	
Entry mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction And blinking of entire display	39us	
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and Blinking of cursor (B) on/off Control bit.		
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display Shift control bit, and the Direction, without changing of DDRAM data.	39us	
Function set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-Bit/4-bit), numbers of display Line (N: =2-line/1-line) and, Display font type (F: 5x11/5x8)	39us	
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address Counter.	39us	
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address Counter.	39us	
Read busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal Operation or not can be known By reading BF. The contents of Address counter can also be read.	0us	
Write data to Address	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us	
Read data From RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us	

### NOTE:

When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2fosc is necessary for executing the next instruction by the falling edge of the “E” signal after the busy flag (DB7) goes to “Low”.

**Contents****1) Clear display**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter).

Return cursor to the original status, namely, bring the cursor to the left edge on the fist line of the display.

Make the entry mode increment (I/D=“High”).

**2) Return home**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return home is cursor return home instruction.

Set DDRAM address to “00H” into the address counter.

Return cursor to its original site and return display to its original status, if shifted.

Contents of DDRAM does not change.

**3) Entry mode set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

**I/D: increment / decrement of DDRAM address (cursor or blink)**

When I/D=“high”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D=“Low”, cursor/blink moves to left and DDRAM address is increased by 1.

\*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

**SH: shift of entire display**

When DDRAM read (CGRAM read/write) operation or SH=“Low”, shifting of entire display is not performed. If SH = “High” and DDRAM write operation, shift of entire display is performed according to I/D value. (I/D=“high”. shift left, I/D=“Low”. Shift right).

**4) Display ON/OFF control**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

**D: Display ON/OFF control bit**

When D=“High”, entire display is turned on.

When D=“Low”, display is turned off, but display data remains in DDRAM.

**C: cursor ON/OFF control bit**

When D=“High”, cursor is turned on.

When D=“Low”, cursor is disappeared in current display, but I/D register preserves its data.

**B: Cursor blink ON/OFF control bit**

When B=“High”, cursor blink is on, which performs alternately between all the “High” data and display characters at the cursor position.

When B=“Low”, blink is off.

**5) Cursor or display shift**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.

This instruction is used to correct or search display data.

During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.

Note that display shift is performed simultaneously in all the lines.

When display data is shifted repeatedly, each line is shifted individually.

When display shift is performed, the contents of the address counter are not changed.

**Shift patterns according to S/C and R/L bits**

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

**6) Function set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

**DL: Interface data length control bit**

When DL=“High”, it means 8-bit bus mode with MPU.

When DL=“Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data twice.

**N: Display line number control bit**

When N=“Low”, 1-line display mode is set.

When N=“High”, 2-line display mode is set.

**F: Display line number control bit**

When F=“Low”, 5x8 dots format display mode is set.

When F=“High”, 5x11 dots format display mode.

**7) Set CGRAM address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

The instruction makes CGRAM data available from MPU.

**8) Set DDRAM address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N=LOW), DDRAM address is from “00H” to “4FH”. In 2-line display mode (N=High), DDRAM address in the 1st line from “00H” to “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.

**9) Read busy flag & address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether ST7066U is in internal operation or not.

If the resultant BF is “High”, internal operation is in progress and should wait BF is to be LOW, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

**10) Write data to RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set).

RAM set instruction can also determine the AC direction to RAM.

After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

**11) Read data from RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before, read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.

After read operation, address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.

At this time, AC indicates next address position, but only the previous data can be read by the read instruction.

## Standard character pattern

Upper 4bit Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

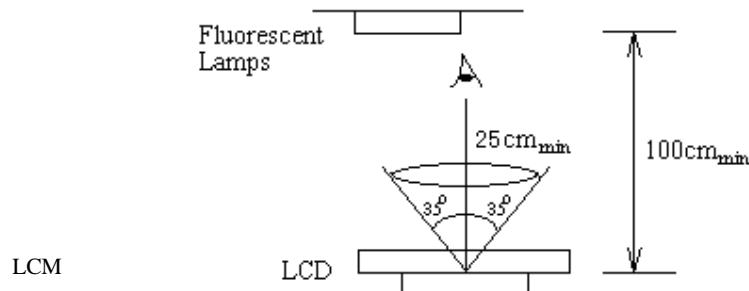
## 11.Quality Specifications

### 11.1 STANDARD OF THE PRODUCT APPEARANCE TEST

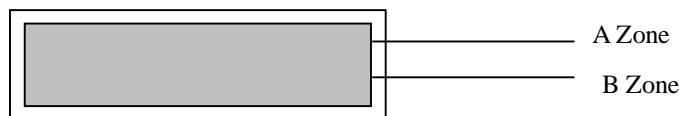
Manner of appearance test: The inspection should be performed in using 20W x 2 fluorescent lamps.

Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 25 cm or more.

Viewing direction for inspection is 35° from vertical against LCM.



Definition of zone:



A Zone: Active display area (minimum viewing area).

B Zone: Non-active display area (outside viewing area).

### 11.2 SPECIFICATION OF QUALITY ASSURANCE

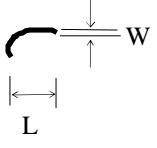
AQL inspection standard

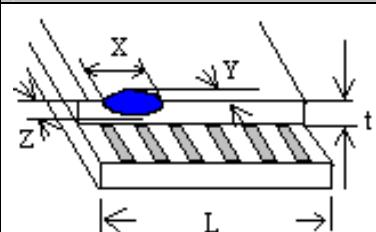
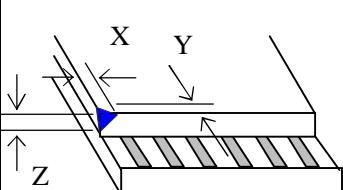
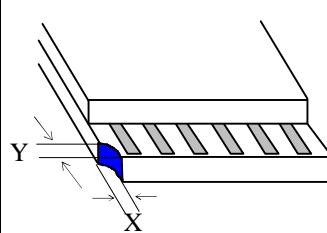
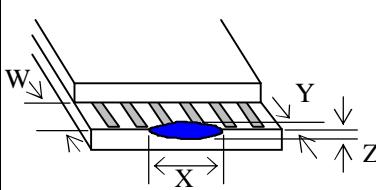
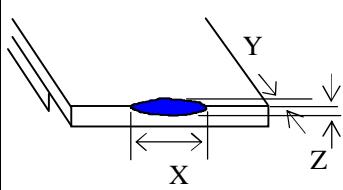
Sampling method: GB2828-87, Level II, single sampling

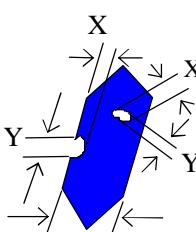
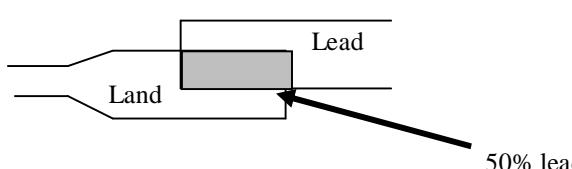
Defect classification (Note: \* is not including)

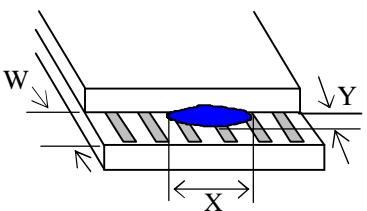
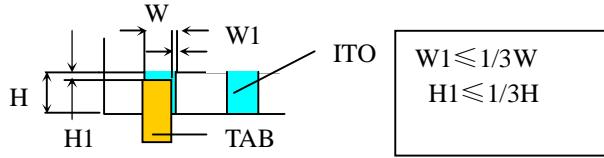
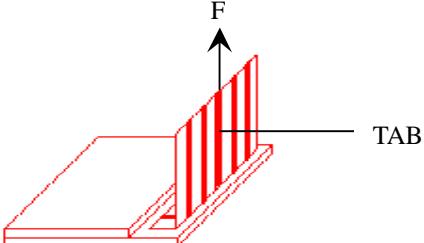
Classify		Item	Note	AQL
Major	Display state	Short or open circuit	1	0.65
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction		
		Contrast defect (dim, ghost)	2	
		Backlight	1,8	
	Non-display	Flat cable or pin reverse	10	1.0
Minor	Display state	Wrong or missing component	11	
		Background color deviation	2	
		Black spot and dust	3	
		Line defect, Scratch	4	
		Rainbow	5	
		Chip	6	
	Polarizer	Pin hole	7	
		Protruded	12	
		Bubble and foreign material	3	
		Soldering	9	
		Wire	10	
		TAB	Position, Bonding strength	13

## Note on defect classification

No.	Item	Criterion													
1	Short or open circuit	Not allow													
	LC leakage														
	Flickering														
	No display														
	Wrong viewing direction														
	Wrong Back-light														
2	Contrast defect	Refer to approval sample													
	Background color deviation														
3	Point defect, Black spot, dust (including Polarizer) $\phi = (X+Y)/2$	 <table border="1"> <thead> <tr> <th>Point Size</th> <th>Acceptable Qty.</th> </tr> </thead> <tbody> <tr> <td><math>\phi \leq 0.10</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.10 &lt; \phi \leq 0.15</math></td> <td>2</td> </tr> <tr> <td><math>0.15 &lt; \phi \leq 0.25</math></td> <td>1</td> </tr> <tr> <td><math>\phi &gt; 0.25</math></td> <td>0</td> </tr> </tbody> </table>	Point Size	Acceptable Qty.	$\phi \leq 0.10$	Disregard	$0.10 < \phi \leq 0.15$	2	$0.15 < \phi \leq 0.25$	1	$\phi > 0.25$	0			
Point Size	Acceptable Qty.														
$\phi \leq 0.10$	Disregard														
$0.10 < \phi \leq 0.15$	2														
$0.15 < \phi \leq 0.25$	1														
$\phi > 0.25$	0														
4	Line defect, Scratch	 <table border="1"> <thead> <tr> <th colspan="2">Line</th> <th>Acceptable Qty.</th> </tr> <tr> <th>L</th> <th>W</th> <td></td> </tr> </thead> <tbody> <tr> <td>---</td> <td><math>0.05 &gt; W</math></td> <td rowspan="4">Disregard</td> </tr> <tr> <td><math>3.0 &gt; L</math></td> <td><math>0.1 &gt; W &gt; 0.05</math></td> </tr> <tr> <td><math>2.0 &gt; L</math></td> <td><math>0.15 \geq W &gt; 0.1</math></td> </tr> </tbody> </table>	Line		Acceptable Qty.	L	W		---	$0.05 > W$	Disregard	$3.0 > L$	$0.1 > W > 0.05$	$2.0 > L$	$0.15 \geq W > 0.1$
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5	Rainbow	Not more than two color changes across the viewing area.													

No	Item	Criterion																														
6	Chip	<p>Remark: X: Length direction Y: Short direction Z: Thickness direction t: Glass thickness W: Terminal width L: Glass length</p>  <p>Acceptable criterion</p> <table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td><math>&lt; L/8</math></td> <td>0.5mm</td> <td><math>\leq t/2</math></td> </tr> </table>  <p>Acceptable criterion</p> <table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td><math>\leq 2</math></td> <td>0.5mm</td> <td><math>\leq t</math></td> </tr> </table>  <p>Acceptable criterion</p> <table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td><math>\leq 3</math></td> <td><math>\leq 2</math></td> <td><math>\leq t</math></td> </tr> </table> <p>shall not reach to ITO</p>  <p>Acceptable criterion</p> <table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>Disregard</td> <td><math>\leq 0.2</math></td> <td><math>\leq t</math></td> </tr> </table>  <p>Acceptable criterion</p> <table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td><math>\leq 5</math></td> <td><math>\leq 2</math></td> <td><math>\leq t/3</math></td> </tr> </table>	X	Y	Z	$< L/8$	0.5mm	$\leq t/2$	X	Y	Z	$\leq 2$	0.5mm	$\leq t$	X	Y	Z	$\leq 3$	$\leq 2$	$\leq t$	X	Y	Z	Disregard	$\leq 0.2$	$\leq t$	X	Y	Z	$\leq 5$	$\leq 2$	$\leq t/3$
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No.	Item	Criterion								
7	Segment pattern W = Segment width $\phi = (X+Y)/2$	<p>(1) Pin hole <math>\phi &lt; 0.10\text{mm}</math> is acceptable.</p>  <table border="1" data-bbox="864 464 1289 633"> <thead> <tr> <th>Point Size</th><th>Acceptable Qty</th></tr> </thead> <tbody> <tr> <td><math>\phi \leq 1/4W</math></td><td>Disregard</td></tr> <tr> <td><math>1/4W &lt; \phi \leq 1/2W</math></td><td>1</td></tr> <tr> <td><math>\phi &gt; 1/2W</math></td><td>0</td></tr> </tbody> </table> <p>Unit: mm</p>	Point Size	Acceptable Qty	$\phi \leq 1/4W$	Disregard	$1/4W < \phi \leq 1/2W$	1	$\phi > 1/2W$	0
Point Size	Acceptable Qty									
$\phi \leq 1/4W$	Disregard									
$1/4W < \phi \leq 1/2W$	1									
$\phi > 1/2W$	0									
8	Back-light	<p>(1) The color of backlight should be in match with the specification.</p> <p>(2) Not allow flickering</p>								
9	Soldering	<p>(1) Not allow heavy dirty and solder ball on PCB. (The size of dirty refer to point and dust defect)</p> <p>(2) Over 50% of lead should be soldered on Land.</p> 								
10	Wire	<p>(1) Copper wire should not be rusted</p> <p>(2) Not allow crack on copper wire connection.</p> <p>(3) Not allow reversing the position of the flat cable.</p> <p>(4) Not allow exposed copper wire inside the flat cable.</p>								
11*	PCB	<p>(1) Not allow screw rust or damage.</p> <p>(2) Not allow missing or wrong putting of component.</p>								

No	Item	Criterion
12	Protruded W: Terminal Width	 <p>Acceptable criteria: <math>Y \leq 0.4</math></p>
13	TAB	<p>1. Position</p>  <p><math>W_1 \leq 1/3W</math> <math>H_1 \leq 1/3H</math></p> <p>2 TAB bonding strength test</p>  <p><math>P (=F/TAB \text{ bonding width}) \geq 650 \text{ gf/cm}</math>, (speed rate: 1mm/min) 5pcs per SOA (shipment)</p>
14	Total no. of acceptable Defect	<p>A. Zone</p> <p>Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm</p> <p>B. Zone</p> <p>It is acceptable when it is no trouble for quality and assembly in customer's end product.</p>

### 11.3 RELIABILITY OF LCM

Reliability test condition:

Item	Condition	Time (hrs)	Assessment
High temp. Storage	80°C	48	No abnormalities in functions and appearance
High temp. Operating	70°C	48	
Low temp. Storage	-30°C	48	
Low temp. Operating	-20°C	48	
Humidity	40°C/ 90%RH	48	
Temp. Cycle	0°C ← 25°C → 50°C (30 min ← 5 min → 30min)	10cycles	

Recovery time should be 24 hours minimum. Moreover, functions, performance and appearance shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature ( $20\pm8^\circ\text{C}$ ), normal humidity (below 65% RH), and in the area not exposed to direct sun light.

## 11.4 PRECAUTION FOR USING LCD/LCM

LCD/LCM is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification.

The followings should be noted.

### GENERAL PRECAUTIONS:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isopropyl alcohol, ethyl alcohol or trichlorotrifloroethane, do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting XIAMEM OCULAR
5. When mounting a LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and also cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal spreads to skin or clothes, wash it off immediately with soap and water.

### STATIC ELECTRICITY PRECAUTIONS:

1. CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.

4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
5. Only properly grounded soldering irons should be used.
6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7. The normal static prevention measures should be observed for work clothes and working benches.
8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

### **SOLDERING PRECAUTIONS:**

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.
3. Soldering temperature:  $280^{\circ}\text{C} \pm 10^{\circ}\text{C}$
4. Soldering time: 3 to 4 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

### **OPERATION PRECAUTIONS:**

1. The viewing angle can be adjusted by varying the LCD driving voltage  $V_o$ .
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. For long-term storage over  $40^{\circ}\text{C}$  is required, the relative humidity should be kept below 60%, and avoid direct sunlight.